CLAIMS

What is claimed is:

| 1 | 1. An integrated circuit (IC) comprising: |
|----|-------------------------------------------------------------------------------------------|
| 2 | a plurality of functional units selectively communicating with each other; |
| 3 | a plurality of logic circuits connected together in ones of said plurality of |
| 4 | functional units, connected said logic circuits in each of said ones defining function |
| 5 | therein; |
| 6 | selectable supply switching devices disposed at ones of said logic circuits |
| 7 | selectively supplying power and alternately isolating connected said logic circuits, said |
| 8 | selectable supply switching devices turning on at a threshold voltage having a magnitude |
| 9 | greater than like devices is said logic circuits; and |
| 10 | a switchable bias supply at each selectable supply switching device selectively |
| 11 | reducing threshold voltage magnitude responsive to said each selectable supply switching |
| 12 | device supplying power. |
| | |
| 1 | 2. An IC as in claim 1, wherein said devices are field effect transistors (FETs), ones |
| 2 | of said selectable supply switching devices are p-type FETs (PFETs) connected between |
| 3 | a supply line (V_{dd}) and an intermediate supply line. |
| | |
| 1 | 3. An IC as in claim 2, wherein whenever ones of said selectable supply switching |

4. An IC as in claim 3, wherein whenever ones of said selectable supply switching devices are isolating said connected logic circuits, said switchable bias supply at said ones provides a body bias of V_{dd} to said one, whereby leakage current in and off said one

devices are supplying power to said connected logic circuits, said switchable bias supply

at said ones provides a body bias of V_{dd} - 0.7V to said one.

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- 4 is substantially reduced with said body bias of V_{dd} over said off ones with body bias at
- 5 $V_{dd} = 0.7V$.
- 1 5. An IC as in claim 2, wherein at least one said intermediate supply line is
- 2 connected to two or more of said logic circuits.
- 1 6. An IC as in claim 2, further comprising a decoupling capacitor at each said
- 2 intermediate supply line.
- 7. An integrated circuit (IC) comprising:
- 2 a plurality of functional units selectively communicating with each other;
- 3 a plurality of logic circuits connected together in each of said plurality of
- 4 functional units, connected said logic circuits in each functional unit defining function in
- 5 said each unit; and
- 6 selectable supply switching devices disposed at ones of said logic circuits
- 7 selectively alternately supplying power and isolating connected said logic circuits, said
- 8 selectable supply switching devices being a high threshold device turning on at a
- 9 threshold voltage having a magnitude greater than at least one like devices is said logic
- 10 circuits, each said of selectable supply switching devices being one in a series of stacked
- 11 high threshold devices.
- 8. An IC as in claim 7, wherein said devices are field effect transistors (FETs), ones
- 2 of said selectable supply switching devices are p-type FETs (PFETs) connected between
- 3 a supply line (V_{dd}) and an intermediate supply line.
- 1 9. An IC as in claim 8, wherein said selectable supply switching PFETs are each one
- of a pair series of stacked said high threshold PFETs, one of each of said pairs being
- 3 connected to V_{dd} and the other of said pair being connected to said intermediate supply
- 4 line.

- 1 10. An IC as in claim 9, wherein at least one said intermediate supply line is
- 2 connected to two or more of said logic circuits.
- 1 An IC as in claim 8, further comprising a decoupling capacitor at each said
- 2 intermediate supply line.
- 1 12. An IC as in claim 8, wherein remaining ones of said selectable supply switching
- devices are n-type FETs (PFETs) connected between a supply return line (Gnd) and an
- 3 intermediate return line.
 - 14. An IC as in claim 12, wherein said series stacked said high threshold devices
- 2 comprises:

- a plurality of high threshold PFET pairs, a first PFET of each of said PFET pairs
- 4 being connected between V_{dd} and said intermediate supply line; and
- 5 a plurality of high threshold NFET pairs, a first NFET of each of said pairs being
- 6 connected between Gnd and said intermediate return line.
- 1 15. An IC as in claim 14, wherein ones of said first PFET are paired with a plurality
- 2 of second PFETs.
- 1 16. An IC as in claim 14, wherein ones of said first NFET are paired with a plurality
- of second NFETs.
- 1 17. An IC as in claim 14, wherein a second PFET of said plurality of high threshold
- 2 PFET pairs is a logic circuit PFET in one first supply switched logic circuit and a second
- 3 NFET of said plurality of high threshold pairs is a logic circuit NFET in one second
- 4 supply switched logic circuit.

- 1 18. An IC as in claim 17, wherein a logic path in at least one of said plurality of
- 2 functional units comprises alternating first supply switched logic circuits and second
- 3 supply switched logic circuits.
- 1 19. An IC as in claim 7, wherein said devices are field effect transistors (FETs), ones
- 2 of said selectable supply switching devices are n-type FETs (NFETs) connected between
- 3 a supply return line (Gnd) and an intermediate return line.
- 1 20. An IC as in claim 19, wherein said selectable supply switching NFETs are each
- 2 one of a pair series of stacked said high threshold NFETs, one of each of said pairs being
 - connected to Gnd and the other of said pair being connected to said intermediate return
- 4 line.

- 1 21. An IC as in claim 20, wherein at least one said intermediate return line is
- 2 connected to two or more of said logic circuits.
- 1 22. An IC as in claim 19, further comprising a decoupling capacitor at each said
- 2 intermediate supply line.
- 1 23. An IC as in claim 7, wherein series of stacked said high threshold devices are
- 2 tapered widest to narrowest with the widest said high threshold devices being disposed in
- 3 said series nearest to a logic circuit output and the narrowest at supply connections.
- 1 24. An IC as in claim 23, wherein tapered said series of stacked high threshold
- devices have a taper ratio of 4, each said high threshold devices in said tapered series
- 3 being 4 times wider than its next adjacent narrower stacked said device.
- 1 25. An IC as in claim 24, wherein said tapered series of stacked high threshold
- 2 devices comprises 2 said high threshold devices.

- 1 26. A method of designing a series of stacked high threshold devices for reducing 2 circuit leakage, said method comprising the steps of:
- a) selecting an equivalent device width;
 - determining stack height reduction of leakage for a number of stack heights;
 - determining leakage for each of a number of taper ratios, circuit leakage being determined by said stack height and taper ratio;
 - d) determining an delay adder for each of said number of taper ratios;
- e) determining a circuit wake up time for each of said number of taper ratios,
 circuit delay being determined by said delay adder and wakeup time; and
 - selecting an optimum stack height and an optimum taper ratio to minimize circuit leakage and circuit delay.
- A method as in claim 26, before the step (f) of said optimum stack height and said
 optimum taper ratio, said method further comprising the steps of:
- e1) determining an intermediate supply bounce for each of said number of
 taper ratios, said intermediate supply bounce affecting circuit delay; and
- c2) determining an in-stack off voltage for each of said number of taper ratios,
 said in-stack off voltage affecting circuit leakage.
- 1 28. A method as in claim 27, wherein the step (f) comprising empirically relating
- 2 circuit leakage and circuit delay to said equivalent device width (W), stack height (N) and
- 3 taper ratio (T).

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- 1 29. A method as in claim 28, wherein empirically relating circuit leakage and circuit
- 2 delay has the form:
- 3 $t_{delay} = (t_0 N/a W/b)(1 T/c)$ and
- 4 $P_{standby} = (k_0 + k_1 exp(-N^2)) (W/2)^d (j_0 + exp(-T))$, where a, b, c, d, k_0 , k_1 and j_0 are process
- dependent coefficients and t0 is the delay with a single header/footer device.